I CLAIM:

1. An integrated circuit chip having a plurality of contact pads to be connected by reflow attachment to outside parts, comprising:

a deposited layer of nickel/titanium alloy on each of said pads, said alloy having a composition and crystalline structure operable in reversible phase transitions under thermomechanical stress, whereby mechanical strain is absorbed by said alloy layer; and

a layer of solderable metal on said alloy, operable as diffusion barrier after said reflow attachment.

2. The chip according to Claim 1 wherein said alloy has between 55.0 and 56.0 weight% nickel, and between 44.0 and 45.0 weight% titanium.

3. The chip according to Claim 1 wherein said alloy layer has a thickness in the range from about 0.3 to 6.0 μm.

4. The chip according to Claim 1 wherein said alloy layer has been recrystallized after deposition in a temperature range from about 450 to 600 °C for a time period between 4 and 6 min.

5. The chip according to Claim 1 wherein said crystalline structure is martensite, having a Lower Superelastic Plateau Stress which is lower than the yield stress of said reflow attachment to outside parts.

6. The chip according to Claim 1 wherein said martensite crystalline structure deforms, upon application of thermally-induced mechanical stress, by twinning, thus avoiding the yielding of said reflow attachment, and finally converts to austenite, returning back to

martensite after removal of said thermomechanical stress.

7. The chip according to Claim 1 wherein said reversible phase transitions are operable in the temperature range from -40 to +125 °C.

8. The chip according to Claim 1 wherein said solderable metal layer is made of nickel and has a thickness in the range from about 0.3 to 0.7 μm.

9. The chip according to Claim 1 further comprising an outermost layer of noble metal to retain solderability of said solderable metal layer, said noble metal layer to be dissolved in said reflow attachment process of said chip to said external part.

10. The chip according to Claim 9 wherein said noble metal is selected from a group consisting of palladium, gold, silver, and alloys thereof, in the thickness range from about 3 to 20 nm.

11. The chip according to Claim 1 wherein said chip has a protective overcoat layer, wherein said plurality of contact pads are opened into said overcoat, exposing the chip metallization.

12. The chip according to Claim 11 wherein said chip metallization is copper-doped aluminum.

13. The chip according to Claim 11 wherein said chip metallization is copper or copper alloy.

14. The chip according to Claim 11 further comprising a layer of refractory metal between said chip metallization and said alloy layer to ensure adhesion of said alloy layer to said protective overcoat.

15. The chip according to Claim 14 wherein said refractory metal is selected from a group consisting of titanium, tungsten, chromium, molybdenum, and alloys thereof.

16. The chip according to Claim 1 further comprising interconnectors operable to assemble said chip onto said outside part.

17. The chip according to Claim 16 wherein said interconnectors are reflowable bumps made of tin, indium, tin alloys including tin/indium, tin/silver, tin/bismuth, tin/lead, conductive adhesives, or z-axis conductive materials.

18. The chip according to Claim 1 wherein said outside parts comprise printed circuit boards, flexible substrates, or any other suitable substrate material.

19. A metallurgical interconnection attaching an electronic device having first coefficient of thermal expansion to an outside body having second coefficient of thermal expansion, comprising:

an electronic device having a plurality of contact pads exposing the device metallization;

each of said contact pads having a layer of nickel/titanium alloy deposited over said device metallization, followed by a solderable nickel barrier layer;

a solder bump attached to said solderable layer of each contact pad;

said outside body having a plurality of terminal pads located in positions respective to said device contact pads, said terminals exposing the metallization of said outside body;

said device attached to said outside body so that said contact pads are aligned with said respective terminal pads, whereby a plurality of metallurgical interconnections are formed operable to absorb, in said nickel/titanium

layer, strain caused by thermomechanical stress due to the difference between said first and second coefficients of thermal expansion.

20. A metallurgical interconnection attaching an outside body having first coefficient of thermal expansion to an electronic device having second coefficient of thermal expansion, comprising:

an outside body having a plurality of terminal pads exposing the body metallization;

each of said terminal pads having a layer of nickel/titanium alloy deposited over said body metallization, followed by a solderable barrier layer;

a solder bump attached to said solderable layer of each terminal pad;

said electronic device having a plurality of contact pads located in positions respective to said body terminal pads, said contacts exposing the metallization of said device;

said device attached to said outside body so that said contact pads are aligned with said respective terminal pads, whereby a plurality of metallurgical interconnections are formed operable to absorb, in said nickel/titanium layer, strain caused by thermomechanical stress due to the difference between said first and second coefficients of thermal expansion.

21. A method of fabricating integrated circuit chips having a plurality of contact pads to be connected by reflow attachment to outside parts, comprising the steps of:

depositing a layer of nickel/titanium alloy composed of 55.5 ± 0.5 weight% nickel and 44.5 ± 0.5

weight% titanium in the thickness range of 0.3 to 6.0 μm;

recrystalling said alloy layer at 500 °C for about 5 min, creating a crystalline structure operable in reversible phase transitions under thermo-mechanical stress, whereby mechanical strain is absorbed by said alloy layer;

depositing a layer of solderable metal on said alloy; and

patterning said deposited layers.

22. The method according to Claim 21 wherein said step of depositing is a DC sputter technique at about 160 W/in² for about 1 hour.

23. The method according to Claim 21 wherein said solderable metal is nickel, deposited by a plating or sputtering technique in a thickness of about 0.5 μm.

24. The method according to Claim 21 further comprising the step of depositing, by electroplating, an outermost layer of palladium in the thickness of about 0.02 μm.